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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/525,203	02/22/2005	Yuichi Takagi	SON-2815	7661

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EXAMINER	
JOSEPH, DENNIS P	

ART UNIT	PAPER NUMBER
2629	

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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/525,203	TAKAGI ET AL.	
	Examiner	Art Unit	
	DENNIS P. JOSEPH	2629	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *21 May 2009*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-4,6-14 and 16-28* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-4, 6-14 and 16-28* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *22 February 2005* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

1. This Office Action is responsive to arguments for application No. 10/525,203 on May 21, 2009. Claims 1-4, 6-14 and 16-28 are pending and have been examined.

Allowable Subject Matter

2. **Claims 1, 2, 4, 6-10 and 12-14 and 16-28** allowed.

Claim Rejections – 35 USC § 103

3. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 103(a) that forms the basis for the rejections under this section made in this Office action:
(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

The factual inquiries set forth in *Graham* **v.** *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:
1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

4. **Claims 3 and 11** rejected under 35 U.S.C. 103(a) as being unpatentable over Yamaguchi (6,332,661) in view of Hughes et al. (US 6,313,780 B1)

Yamaguchi teaches in Claim 3:

A current output type drive circuit for outputting a drive current to a driven object shared by being divided into a plurality of areas **(Figure 1 shows the current drivers used to drive the EL devices 51, 52, etc (read as a plurality of areas))**,

comprising a plurality of drivers arranged corresponding to each the shared area of the driven object **(Figure 1, driver ICS 1, 2 and 3, Column 5, Lines 41-46)**,

each driver comprising

an output means for outputting a supplied reference current and the drive current corresponding to image data to a corresponding shared area of the driven object **(Figure 1, output terminals 001-064, Column 5, Lines 41-46. The terminals output the current from the driver circuits to the pixel elements)** and

a reference current source circuit **(Figure 1, reference current generation circuit 12. It is connected to each driver)**, but

Yamaguchi does not explicitly teach the reference current source circuit is used "for sampling and holding the reference current input from a reference current input terminal, then supplying the same to the output means."

However, sampling and holding circuitry and means is well known in the art, in conjunction with current mirrors, taught by Yamaguchi and disclosed in Figure 3, which shows circuitry within the reference current generation circuit 12. In addition, Yamaguchi teaches of the reference current input terminals IREF as shown in Figures 1 and 2.

To emphasize on this, in the same field of endeavor, current circuitry, Hughes teaches of using current memories M41 and M42 to sample and hold the input current sample, (Hughes, Column 2, Lines 35-48). During the four phases, the two memories sample and store (read as held) and then outputted accordingly. The reference terminals of Yamaguchi connect to the reference current generation circuit 12 and the sampling and holding means are processed within 12 and then output accordingly.

Therefore, it would be obvious to one of ordinary skill at the time of the invention to integrate the sampling and holding means by using the current memories, as taught by Hughes, with Yamaguchi's circuitry, with the motivation that is sampling and holding is a well known technique in the art. KSR teachings provide many principles here, such as known technique, simple substitution of parts, with regards to implementing the circuitry, suggestion in the prior art, Yamaguchi, etc. Applicant has also noted that this is well known as well. As for implementing them with the current memories, Hughes notes that by using two memories, data will not be corrupted, so data loss can be prevented, (Hughes, Column 2, Lines 4-19)

Yamaguchi also does not explicitly teach "a current sampling circuit including a current memory for sampling and holding said reference current in accordance with a control signal," "a control circuit for outputting to said current sampling circuit a control signal for controlling write and read operations of said reference current of the current memory of said current sampling circuit," "wherein said current sampling circuit includes a fist current memory and a second current memory," and "said control circuit outputs to said current sampling circuit said control signal so

as to alternately perform a write operation of the reference current input from said reference current input terminal and a read operation of the written reference current on said first current memory and second current memory."

However, Hughes teaches in Figure 4 of first and second current memories M41 and M42. Figure 4 also shows the switches for each memory. It is obvious to one of skill that there is a control means for controlling the functionality of the process of the current memories as disclosed in Column 2, Lines 35-48. It is obvious to one of skill that there is a control means for controlling the functionality of the process of the current memories as disclosed in Column 2, Lines 35-48. As for the alternating manner between reading and writing, this section discloses that during a first phase, there is writing to a first current memory, during a second phase, there is writing to the second memory while reading from the first memory and this repeats. This shows an alternating manner between the reading and writing operation. The combination with Yamaguchi teaches of using the sampling and holding circuit, including these memories, within the reference current generation circuit 12.

Therefore it would be obvious to one of ordinary skill in the art at the time of the invention to integrate the current memories, as taught by Hughes, with Yamaguchi's reference current generation circuit with the motivation, that as discussed above, Hughes notes that by using two memories, data will not be corrupted, so data loss can be prevented, (Hughes, Column 2, Lines 4-19).

Yamaguchi teaches in Claim 11:

A current output type drive circuit for outputting a drive current to a driven object shared by being divided into a plurality of areas **(Figure 1 shows the current drivers used to drive the EL devices 51, 52, etc (read as a plurality of areas))** comprising a plurality of drivers arranged corresponding to each of the shared area of the driven object **(Figure 1, driver ICS 1, 2 and 3, Column 5, Lines 41-46)**,

each driver comprising

an output means for outputting a supplied reference current as a drive current to the corresponding shared area of the driven object **(Figure 1, output terminals 001-064, Column 5, Lines 41-46. The terminals output the current from the driver circuits to the pixel elements)** and

a reference current source circuit **(Figure 1, reference current generation circuit 12. It is connected to each driver)** for sampling and holding a reference current input from a reference current input terminal, then supplying the same to the output means,

the reference current input terminal being connected to a reference current input terminal of another driver by a common current interconnect **(Figure 1, the reference current generation circuit 12 branches and inputs to each of the drivers. The common interconnect is shown in Figure 1 which connects the reference current generation circuit 12 which sends multiple current lines to the current driver circuits)**, and

the reference current being distributed to the reference current source circuits of the drivers by time division **(Figure 1 of Yamaguchi shows a reference current generation circuit 12 which is used to send various signals to each of the drivers)**,

wherein said reference current source circuit **(Figure 1, the reference current generation circuit 12)**; but

Yamaguchi does not explicitly teach the reference current source circuit is used "for sampling and holding the reference current input from a reference current input terminal, then supplying the same to the output means."

However, sampling and holding circuitry and means is well known in the art, in conjunction with current mirrors, taught by Yamaguchi and disclosed in Figure 3, which shows circuitry within the reference current generation circuit 12. In addition, Yamaguchi teaches of the reference current input terminals IREF as shown in Figures 1 and 2.

To emphasize on this, in the same field of endeavor, current circuitry, Hughes teaches of using current memories M41 and M42 to sample and hold the input current sample, (Hughes, Column 2, Lines 35-48). During the four phases, the two memories sample and store (read as held) and then outputted accordingly. The reference terminals of Yamaguchi connect to the reference current generation circuit 12 and the sampling and holding means are processed within 12 and then output accordingly.

Therefore, it would be obvious to one of ordinary skill at the time of the invention to integrate the sampling and holding means by using the current memories, as taught by Hughes, with Yamaguchi's circuitry, with the motivation that is sampling and holding is a well known

technique in the art. KSR teachings provide many principles here, such as known technique, simple substitution of parts, with regards to implementing the circuitry, suggestion in the prior art, Yamaguchi, etc. Applicant has also noted that this is well known as well. As for implementing them with the current memories, Hughes notes that by using two memories, data will not be corrupted, so data loss can be prevented, (Hughes, Column 2, Lines 4-19)

Yamaguchi also does not explicitly teach "a current sampling circuit including a current memory for sampling and holding said reference current in accordance with a control signal," "a control circuit for outputting to said current sampling circuit a control signal for controlling write and read operations of said reference current of the current memory of said current sampling circuit," "wherein said current sampling circuit includes a fist current memory and a second current memory," and "said control circuit outputs to said current sampling circuit said control signal so as to alternately perform a write operation of the reference current input from said reference current input terminal and a read operation of the written reference current on said first current memory and second current memory."

However, Hughes teaches in Figure 4 of first and second current memories M41 and M42. Figure 4 also shows the switches for each memory. It is obvious to one of skill that there is a control means for controlling the functionality of the process of the current memories as disclosed in Column 2, Lines 35-48. It is obvious to one of skill that there is a control means for controlling the functionality of the process of the current memories as disclosed in Column 2, Lines 35-48. As for the alternating manner between reading and writing, this section discloses

that during a first phase, there is writing to a first current memory, during a second phase, there is writing to the second memory while reading from the first memory and this repeats. This shows an alternating manner between the reading and writing operation. The combination with Yamaguchi teaches of using the sampling and holding circuit, including these memories, within the reference current generation circuit 12.

Therefore it would be obvious to one of ordinary skill in the art at the time of the invention to integrate the current memories, as taught by Hughes, with Yamaguchi's reference current generation circuit with the motivation, that as discussed above, Hughes notes that by using two memories, data will not be corrupted, so data loss can be prevented, (Hughes, Column 2, Lines 4-19).

Response to Arguments

5. Applicant's arguments have been considered, but are respectfully not persuasive.

Applicant is thanked for incorporating objected material into the independent claim and as a result, the claims which have the objected material have now been allowed.

Applicant's arguments with respect to Claims 3 and 11 are respectfully not persuasive. The claim language, as examiner interprets it, recites that there is an alternating operation performed with regards to the reading and writing function using two current memories. This is what Hughes respectfully is teaching though in Column 2, Lines 35-48 when he discloses that during a first phase, for a first current memory, a read phase occurs. Then, in the second phase, a read phase occurs for the second current memory while the writing phase occurs for the first

current memory. It then discloses that it repeats, which is obvious in the art anyway. The claim language is broad enough to interpret Hughes like this.

Applicant is advised to better claim the alternating process in more detail to overcome the current rejection.

Conclusions

6. Applicant's amendments and non-persuasive arguments necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Dennis P. Joseph whose telephone number is 571-270-1459. The examiner can normally be reached on Monday-Friday, 8am-5pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Amr Awad can be reached on 571-272-7764. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

DJ

/Amr Awad/
Supervisory Patent Examiner, Art Unit 2629